

INDIAN INSTITUTE OF SCIENCE EDUCATION AND RESEARCH THIRUVANANTHAPURAM [IISERTVM]

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Date: 28th July 2015

ADDENDUM - II TO TENDER NO

No: IISER/PUR/5790/15

Dear Sirs,

Sub: HPC Cluster- Responses to Queries

This has reference to the queries from after the date of Addendum – I raised by the Bidders. The responses of IISERTVM are available in Annexure to this Addendum. Vendors are required to make note of these changes to our technical specifications and commercial terms of the tender notice No. IISER/PUR/5790/15 under advertisement No. IISER/PUR/PT/3/15 dated 2/6/2015.

Last date for submission of tender is extended upto 2.00PM on 13th

August 2015 and Tender opening is at 3.00PM on 13th August 2015.

Thanking You,

Yours Faithfully

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Answers to the queries from vendors received after the date of Addendum I [09.07.2015]

TENDER No: IISER/PUR/PT/3/15

SL No	SPECIFICATION REFERENCE	Queries	Response
1	in the Technical bid evaluation.	marks as per your RFP, it is come to 56 & not 65. But the tender mentioned as	This is an intended feature of the scoring scheme (not a typographic error). It means that, a bidder has to secure more than minimum score in some of the individual qualifying criteria in order to secure the overall minimum score of 65.
2	Benchmark program: Sl. No. 1 SCALAPACK matrix inversion using the routine PDGETRI.f. (See RFQ for full specification)	,	The bidder is expected to write their own driver program code for using the routine (and its prerequisite PDGETRF.f) for inversion of the specified matrix.
3	CUDA version of routine PDGETRI.f for running on CPU+GPU cluster	(IISER/PUR/5790/15), scalapack matrix inversion benchmark has to be done on CPU and GPU based system (10 TFlops). We checked with NVIDIA and there is no GPU scaLAPACK version of PDGETRI available. But MAGMA project has a multi-GPU version of PDGETRF (LU factorization routine which is the prerequisite of PDGETRI). It means the PDGETRF will be executed on the GPU whereas the core Inversion routine PDGETRI will be executed on the CPU only.	Benchmark Program Sl No.2: Quantum Espresso: The program "Medium-size benchmark for pw.x" described in "http://qeforge.org/gf/project/q-e/frs/?action=FrsReleaseView&release_id=44" should be run on a CPU+GPU cluster having 10 TFLOPS of Rpeak. The binary "pw.x" should be built with GPU support enabled. Patches for GPU enabled version are available at:

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			purpose.
4	Regarding interconnect Fabric	No IISER/PUR/5790/15, you have removed QDR/Dual Rail from the Infiniband option. By removing QDR from the option, this part of bid has become very proprietary to one particular OEM, thus eliminating competition & giving that particular OEM complete advantage. Request you to consider QDR Dual Rail option & we are open for accepting the benchmark criteria. (HCL): For the primary interconnect, we are allowed to offer FDR/EDR or equivalent with higher bandwidth. FDR bandwidth is 56Gbps. Intel is coming up with a new interconnect called Omniscale. This will be	PART-J of the RFQ is accordingly modified as given below (to be read along with the following statement). NOTE: Since Intel Omni-path is not released yet, vendor may also provide Intel QDR fabric for the time being, however this will have to be upgraded to Intel Omni-path at no extra cost as soon it is available in the market. Written committment for the same with specified time bound for the upgrade should be included in the technical bid. The last stage payment of 10% for demonstrating the performance without reboot after 30 days will NOT be released until the above upgrade of Intel QDR to Intel Omni-path fabric is completed.
	Integrity pact		Integrity Pact may be printed on plain paper and submitted with the seal and signatures of bidder. This should be the part of Technical bid.

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PART-J OF THE RFQ IS MODIFIED AS FOLLOWS PART - J NETWORK / INTERCONNECT								
						Components	SPECIFICATION	
						Interconnect fabric	1)FDR/XDR/equivalent-or-higher infiniband (IB) (in terms of bandwidth) OR Intel Omni-Path Fabric 100 Series, Chassis switch with redundant power supply and redundant fan, HCA/HFI cards, cables, etc. 2) The solution should have fully non-blocking interconnect fabric, with FDR/XDR/ equivalent-or-better IB topology/Intel Omni-Path Fabric 100 Series using a single chassis switch. 3) Management modules in IB/Omni-Path switch should be redundant.	
Management switch (Gigabit LAN switch)	 Master /Head /Login node has to have 10 Gbps NIC for LAN connectivity. All nodes to be connected by Gigabit network for administrative 							
	works.							

NOTE:

- (1) The price bid format should also become part of technical bid **without** price component for complying the tendered configuration. Any deviation/change of the price bid format in price bid cover amounts to disqualification of the vendor.
- (2) Last Date of Submission of Tender is extended upto 2.00 pm on 13th August 2015 and Tender opening is at 3.00 pm on 13th August 2015

Deputy Registrar [Purchase & Stores]